**IN THE CLAIMS:**

1. (Canceled)

2. (Currently Amended) An electronic circuit according to claim [[1]]4, comprising a further power supply reference conductor and a further switching circuit, complementary to the switching circuit, the further switching circuit comprising: a third MOS transistor of the second conductivity type, having a source, a drain and a gate, the source being coupled to the further power supply reference conductor a second MOS transistor of the first conductivity type, with a source, a drain and a gate, the source being coupled to the drain of the third MOS transistor the drain being coupled to the signal conductor or a further signal conductor; the control circuit having outputs coupled to the gate of the third MOS transistor and the gate and source of the fourth MOS transistor the control circuit applying gate source voltages to the third and fourth MOS transistor to make these third and fourth MOS transistors conductive and not to make these transistors conductive respectively.

3. (Original) An electronic circuit according to claim 2, wherein the control circuit is arranged to supply first substantially matching gate-source voltages to the first and fourth MOS transistor and second substantially matching gate-source voltages to the second and third MOS transistor.

4. (Currently Amended) ~~An electronic circuit according to claim 1~~ An electronic circuit, comprising a signal conductor a power supply reference conductor and a

switching circuit coupled between the signal conductor and the power supply reference conductor, the switching circuit comprising: a substrate arrangement coupled to the power supply reference conductor; a first MOS transistor realized on said substrate arrangement with a source, a drain and a gate, the source being coupled to the power supply reference conductor the first MOS transistor having a first conductivity type; a second MOS transistor realized on said substrate arrangement with a source, a drain and a gate, the source being coupled to the drain of the first MOS transistor the drain being coupled to the signal conductor the second MOS transistor having a second conductivity type opposite the first conductivity type; a control circuit with outputs coupled to the gate of the first MOS transistor and the gate and source of the second MOS transistor the control circuit being arranged to switch between an "on" state and an "off" state, in which the control circuit controls the gate source voltages of the first and second MOS transistors to make channels of the first and second MOS transistors conductive and not to make the channels of these first and second MOS transistors conductive respectively;

wherein each of the first and second MOS transistors have source-drain diodes in anti-series so that said first and second MOS transistors have a respective maximum breakdown voltage at drain voltages in mutually opposite directions relative to a substrate voltage, wherein the control circuit comprises: a power supply input for supplying a power supply voltage with a first polarity relative to the power supply reference conductor the first conductivity type being such that the channel of the first MOS transistor becomes conductive when a voltage at its gate has a second polarity, opposite the first polarity relative to its source; a pump circuit fed with the power supply voltage

and arranged to generate the gate voltage of the first MOS transistor with the second polarity relative to the power supply reference conductor in the "on" state.

5. (Currently Amended) ~~An electronic circuit according to claim 1~~ An electronic circuit, comprising a signal conductor a power supply reference conductor and a switching circuit coupled between the signal conductor and the power supply reference conductor, the switching circuit comprising: a substrate arrangement coupled to the power supply reference conductor; a first MOS transistor realized on said substrate arrangement with a source, a drain and a gate, the source being coupled to the power supply reference conductor the first MOS transistor having a first conductivity type; a second MOS transistor realized on said substrate arrangement with a source, a drain and a gate, the source being coupled to the drain of the first MOS transistor the drain being coupled to the signal conductor the second MOS transistor having a second conductivity type opposite the first conductivity type; a control circuit with outputs coupled to the gate of the first MOS transistor and the gate and source of the second MOS transistor the control circuit being arranged to switch between an "on" state and an "off" state, in which the control circuit controls the gate source voltages of the first and second MOS transistors to make channels of the first and second MOS transistors conductive and not to make the channels of the first and second MOS transistors conductive respectively;

wherein each of the first and second MOS transistors have source-drain diodes in anti-series so that said first and second MOS transistors have a respective maximum breakdown voltage at drain voltages in mutually opposite directions relative to a substrate voltage, wherein the control circuit comprises: a power supply input for supplying a

power supply voltage relative to the power supply reference conductor with a first polarity, the second conductivity type being such that the channel of the second MOS transistor becomes conductive when a voltage at its gate has a second polarity, opposite the first polarity relative to its source; a resistive element coupled between the gate and source of the second MOS transistor; a current source circuit coupled between the power supply input and the gate of the second MOS transistor for supplying a predetermined, state dependent current from the power supply input to through the resistive element.

6. (Previously amended) An electronic circuit, comprising a signal conductor a power supply reference conductor and a switching circuit coupled between the signal conductor and the power supply reference conductor, the switching circuit comprising:

a substrate arrangement coupled to the power supply reference conductor; a first MOS transistor realized on said substrate arrangement with a source, a drain and a gate, the source being coupled to the power supply reference conductor the first MOS transistor having a first conductivity type; a second MOS transistor realized on said substrate arrangement with a source, a drain and a gate, the source being coupled to the drain of the first MOS transistor the drain being coupled to the signal conductor the second MOS transistor having a second conductivity type opposite the first conductivity type; a control circuit with outputs coupled to the gate of the first MOS transistor and the gate and source of the second MOS transistor the control circuit being arranged to switch between an "on" state and an "off" state, in which the control circuit controls the gate source voltages of the first and second MOS transistor to make channels of these MOS transistors conductive and not to make the channels of these first and second transistors

conductive respectively wherein the control circuit comprises: a power supply input for supplying a power supply voltage relative to the power supply reference conductor with a first polarity, the second conductivity type being such that the channel of the second MOS transistor becomes conductive when a voltage at its gate has a second polarity, opposite the first polarity relative to its source; a resistive element coupled between the gate and source of the second MOS transistor; a current source circuit coupled between the power supply input and the gate of the second MOS transistor for supplying a predetermined, state dependent current from the power supply input to through the resistive element, and

further comprising a further resistive element and a current mirror circuit with an input branch and an output branch, the further resistive element and the input branch being coupled in series between the power supply reference conductor and the further power supply reference conductor the output branch being coupled to the gate of the second MOS transistor an input/output factor of the current mirror and a ratio between resistance values of the resistive element and the further resistive element having values so that a first voltage drop over the further resistive element is substantially equal to a second voltage drop over the resistive element.

7. (Original)An electronic circuit according to claim 6, wherein the control circuit comprises: a pump circuit fed with the power supply voltage and arranged to generate the gate voltage of the first MOS transistor with the first polarity relative to the power supply reference conductor in the "on" state, the pump circuit comprising junction type pumping diodes, the current mirror comprising bipolar transistors.

8. (Canceled)

9. (Canceled)